Attorney Docket No. 81862.P096

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Gene Chui

Serial No. 09/090,096

Filed: June 3, 1998

For: A METHOD AND APPARATUS

FOR PROVIDING

PROGRAMMABLE MEMORY

FUNCTIONS FOR BI-

DIRECTIONAL TRAFFIC IN A

SWITCH PLATFORM

EXAMINER: LOGSDON, JOSEPH B.

ART UNIT: 2662

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Commissioner for Patents PO Box 1450 Alexandria, Virginia 22313-1450

SUBMISSION OF FORMAL DRAWINGS

Enclosed for filing in the above-referenced patent application are forty five (45) sheets of formal drawings.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: <u>///3</u>, 2005

Daniel E. Ovanezian C Registration No. 41,236

12400 Wilshire Boulevard Seventh Floor Los Angeles, California 90025-1026 (408)720-8300



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Name of Person Mailing Correspondence	1/13/05
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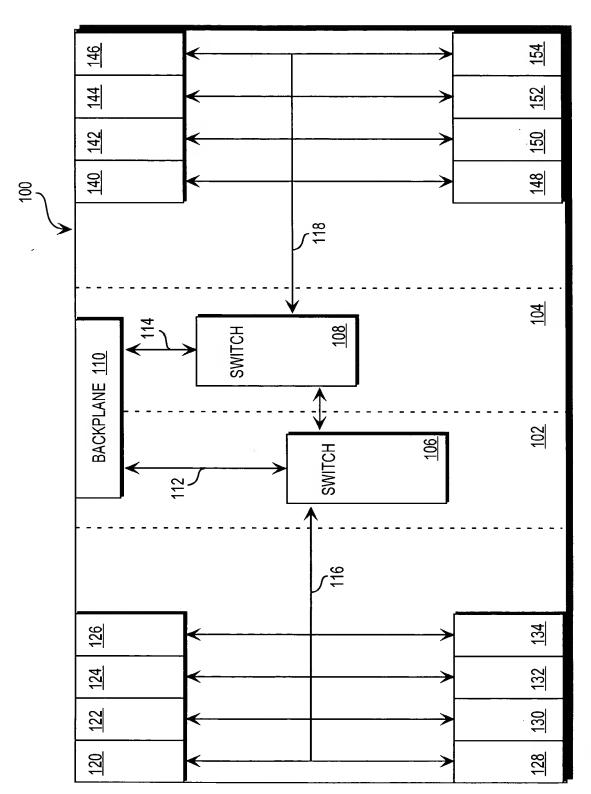


FIG. 1



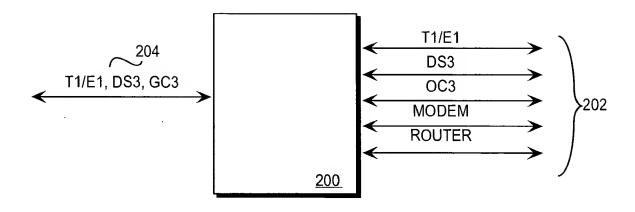
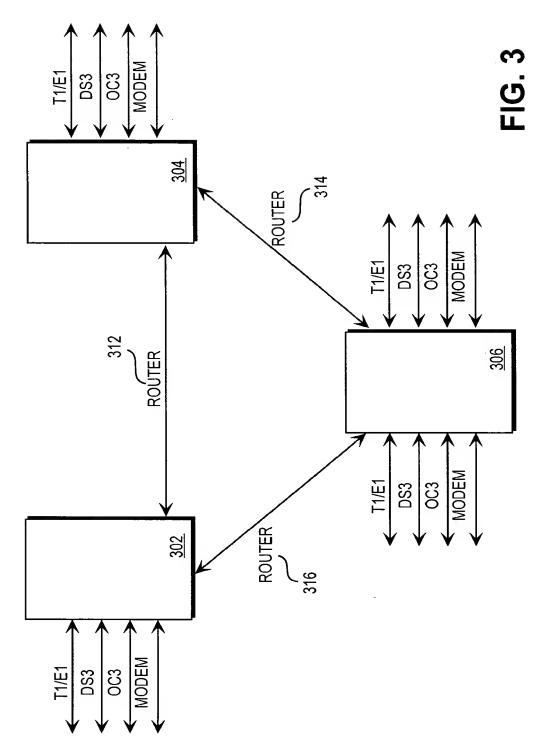
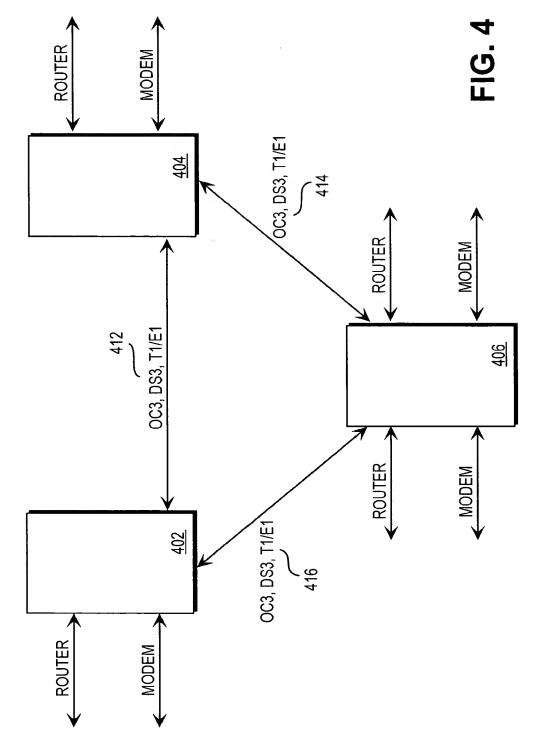


FIG. 2











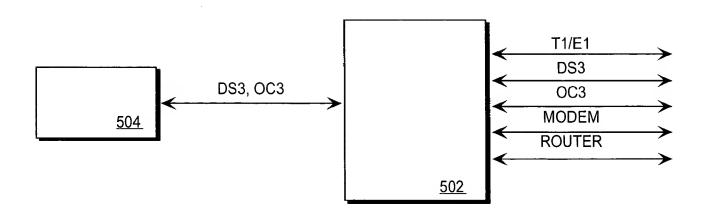


FIG. 5



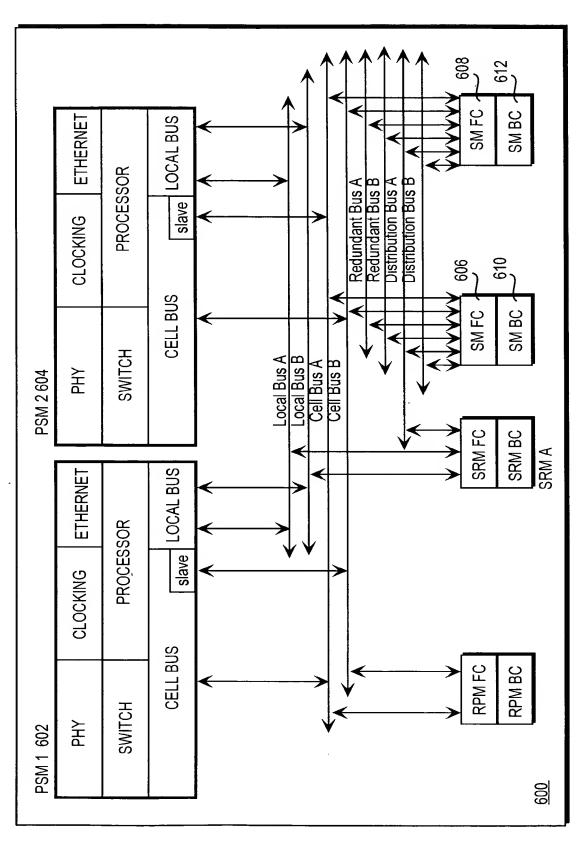


FIG. 6



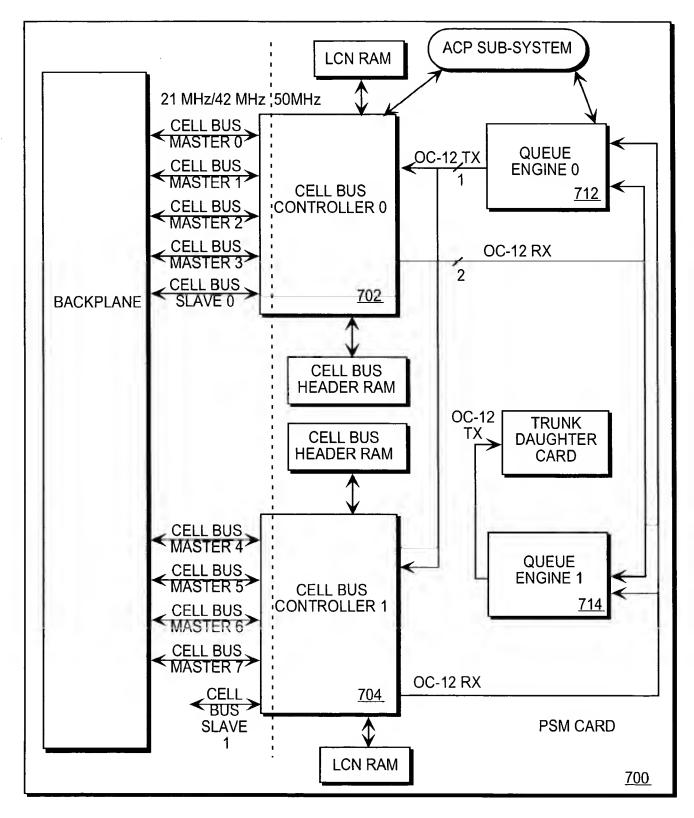


FIG. 7



Р	15	0
	ATM HEADER HWORD 0	
	ATM HEADER HWORD 1	
	LCN	
	DATA HWORD 0	
	DATA HWORD 1	
	•	
	•	
	•	
	DATA HWORD 22	
	DATA HWORD 23	
	P	ATM HEADER HWORD 0 ATM HEADER HWORD 1 LCN DATA HWORD 0 DATA HWORD 1 O DATA HWORD 22

FIG. 8



	Р	7	0
0		CELL BUS HEADER BYTE 0	
1		CELL BUS HEADER BYTE 1	
2		CELL BUS HEADER BYTE 2	
3		CELL BUS HEADER BYTE 3	
4		ATM HEADER BYTE 1	
		•	
		•	
		- ●	
54		DATA BYTE 46	
55		DATA BYTE 47	

FIG. 9



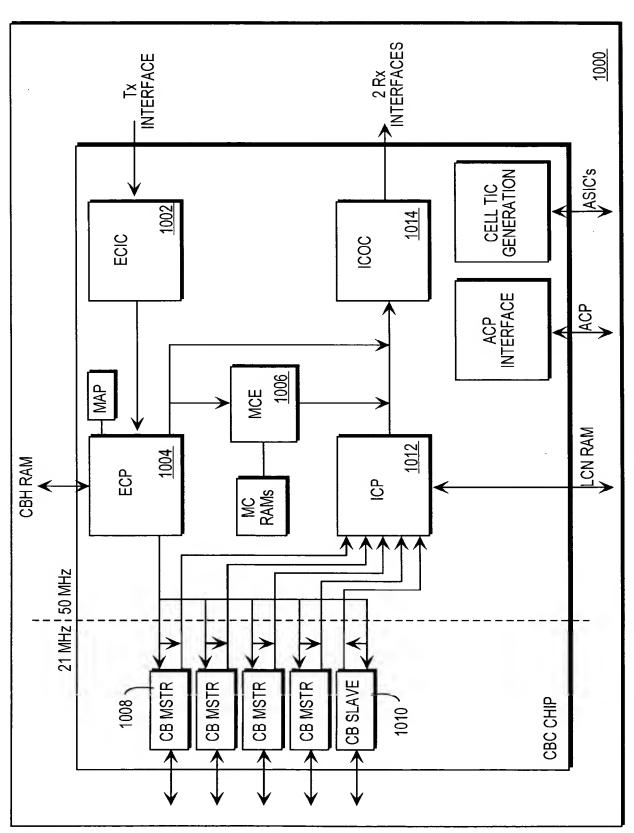


FIG. 10



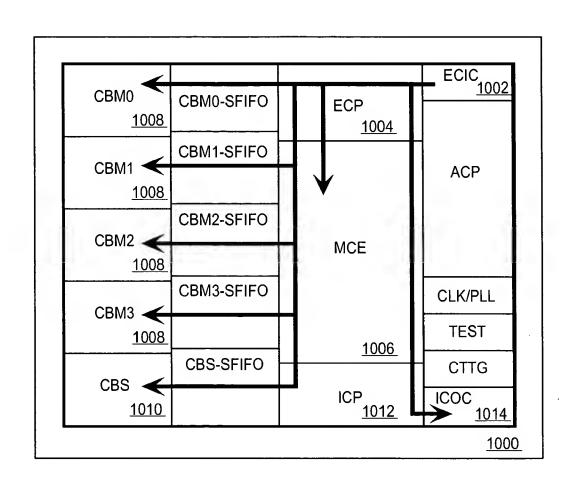


FIG. 11



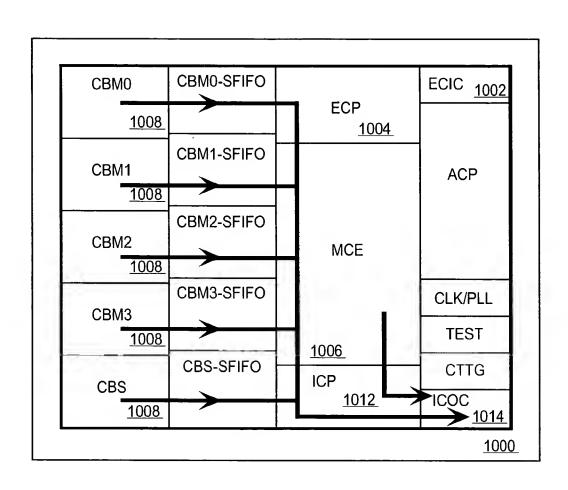


FIG. 12



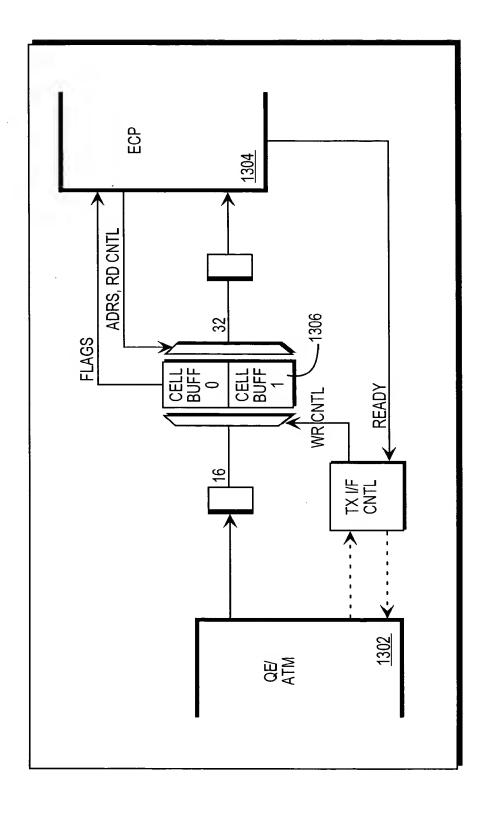


FIG. 13



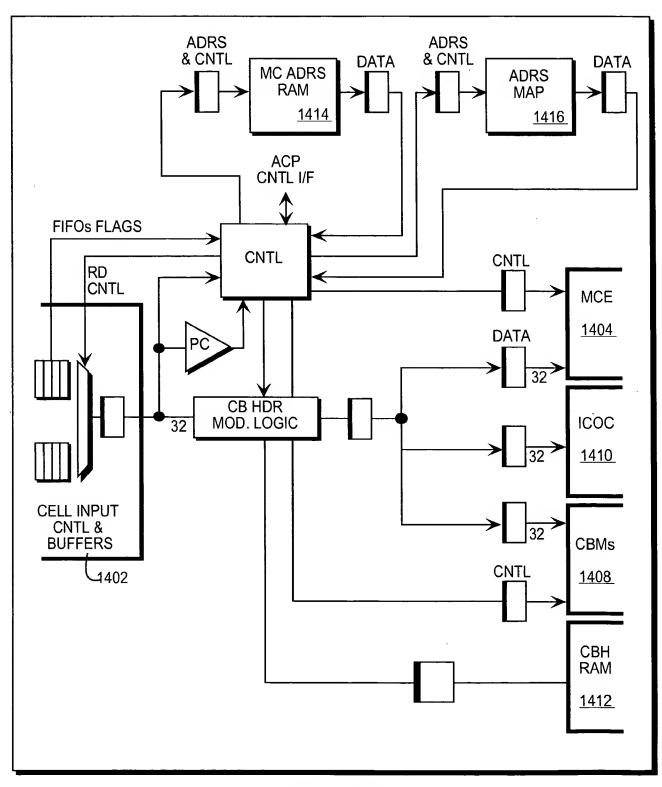


FIG. 14



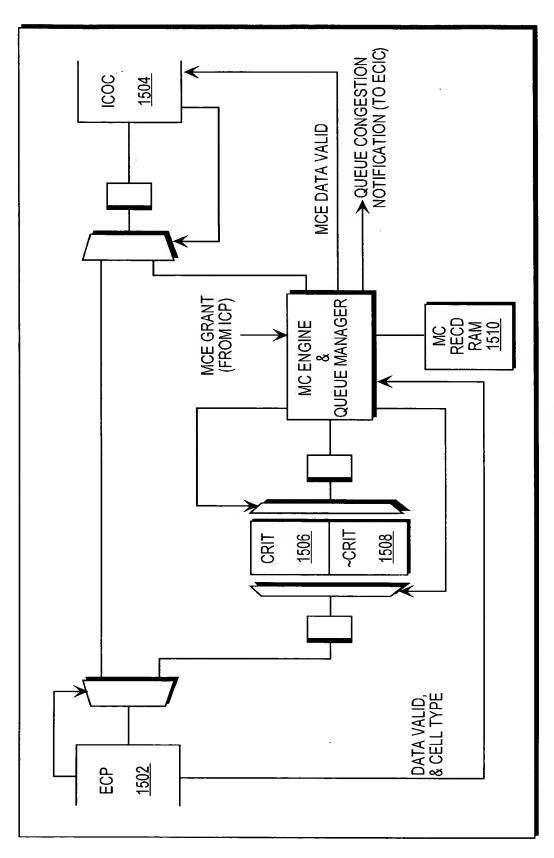


FIG. 15



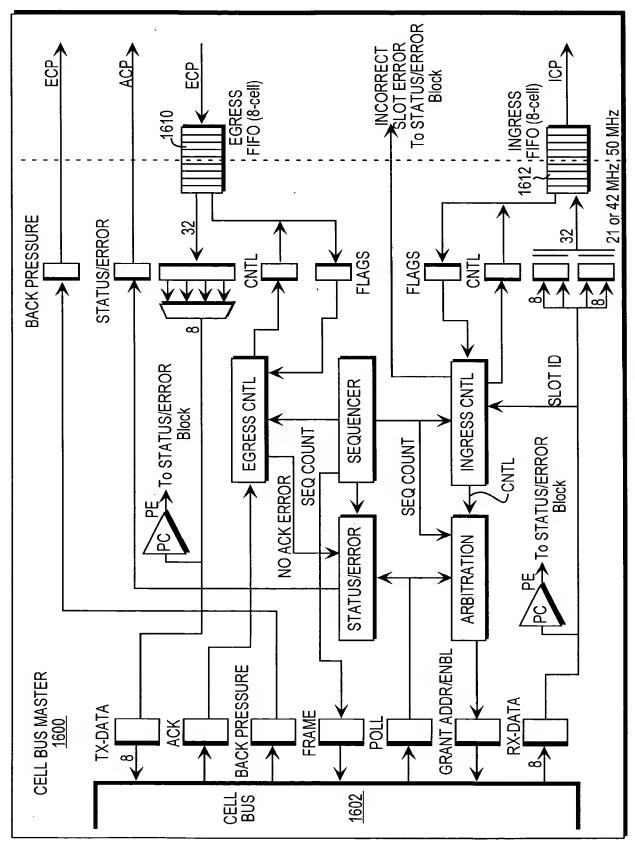


FIG. 16



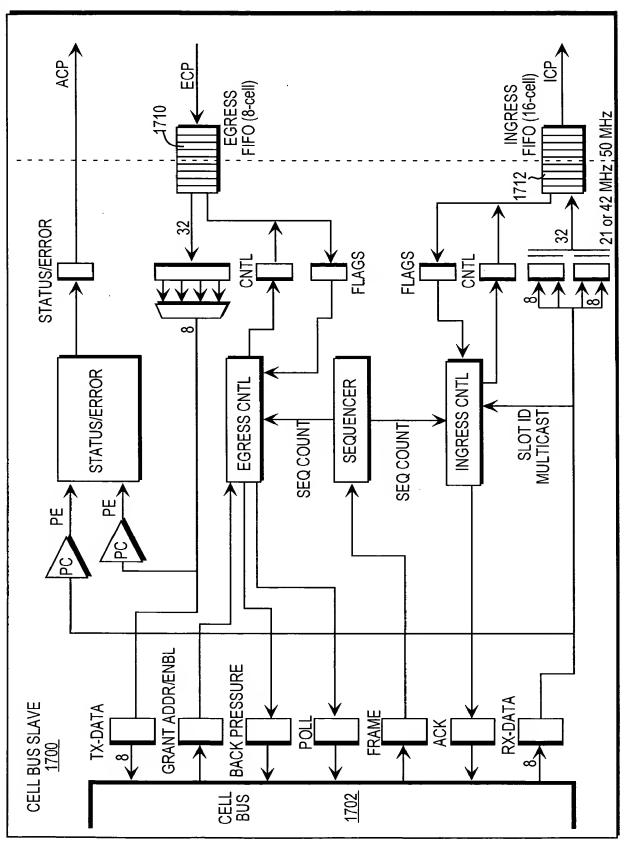


FIG. 17



								-												_)
Ack_Lo			_							0	(CBM	at .	Cycle	(A)						(
Rx Data (From Slave)	0	First Byte	Byte 2	Byte 3	Byte 4	Byte 5	Bytes 6-9	Byte 10	Bytes 11-14	Byte 15	Byte 16	Byte 17	Byte 18	Bytes 19-25	Byte 26	Bytes 27-33	Byte 34	Bytes 35-41	Byte 42	7
Tx Data (To Slave)	First Byte	of Cell	Byte 2	Byte 3	Byte 4	Byte 5	Bytes 6-9	Byte 10	Bytes 11-14	Byte 15	Byte 16	Byte 17	Byte 18	Bytes 19-25	Byte 26	Bytes 27-33	Byte 34	Bytes 35-41	Byte 42	て -)
Reset						0						1							0	(
Grant Enable	-					0					Reset	Туре					0			て ン
Grant Address					0					ō	Slot to Reset						0			~ _)
Poll	0		Odd Request			0	•	Even Request		0			Odd Ready	0	Even Ready	0	Odd Present	0	Even Present	()
TX Frame	_														0					_)
Cell Bus Cycle	0/58	-	2	3	4	ည	6-9	10	11-14	15	16	17	18	19-25	56	27-33	34	35-41	42	て ノ

FIG. 18



)										_	
<u> </u>	Bytes 43-49	Byte 50	Byte 51	Byte 52	Byte 53	Byte 54	Byte 55	Byte 56		0	
	Byte	By	Ву	By	By	By	By	By			
(Bytes 43-49	Byte 50	Byte 51	Byte 52	Byte 53	Byte 54	Byte 55	Byte 56	0	First Byte of	next cell
\ (c	>								
)							-			 <u></u>	
(·		
(Grant				0				
(0	Odd Stop			0			Even Stop		0	
,		•		•						-	_
>	43-49	20	51	52	53	54	55	56	57		28/0
(l		l			1			

FIG. 18 (CONT.)



Cell Bus TX Poll Grant Orant Grant																,					_)	
TX	Ack_Lo	0		7 : 7	7-III																_)	
Frame Poll Address Enable Reset 1 Hi-Z Odd Request Even Request Odd Ready Odd Ready Odd Ready Odd Ready D Hi-Z Slot to Reset Type Type 1 Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Hi-Z Slot to Hi-Z Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Hi-Z Slot to Hi-Z Hi-Z Hi-Z Slot to Hi-Z Slot to Hi-Z Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Hi-Z Hi-Z Hi-Z Slot to Hi-Z Slot to Hi-Z Hi-Z Slot to Hi-Z Hi-Z Hi-Z Slot to Hi-Z Slot to Hi-Z Hi-Z Hi-Z Slot to Hi-Z Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Slot to Hi-Z Hi-Z Slot to Odd Ready D	Rx Data (To CBM)	Hi-Z	First Byte	Byte 2	Byte 3	Byte 4	Byte 5	Bytes 6-8	Byte 9	Byte 10	Byte 11	Bytes 12-14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19	Bytes 20-24	Byte 25	Byte 26)	
Frame Frame Grant Grant Grant I Hi-Z	Tx Data (From CBM)	First Byte	of Cell	Byte 2	Byte 3	Byte 4	Byte 5	Bytes 6-8	Byte 9	Byte 10	Byte 11	Bytes 12-14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19	Bytes 20-24	Byte 25	Byte 26	て	
Frame Frame Address 1 Hi-Z Odd Request Even Ready Odd Ready Odd Ready Odd Ready D Hi-Z Slot to Reset Odd Ready Odd Ready Odd Ready Odd Ready Odd Ready	Reset			•			0								-						(19
Frame 1 Hi-Z Odd Request Even Ready Odd Ready Odd Ready Even Ready	Grant Enable	_					0						-	Reset	lype		•				て 」	FIG.
Fig	Grant Address					0							01+10	Sior to Reset						0	て _)	
 	Poll	Hi-Z		Odd Request			Z-iH		C	Even Kequest		7:11	7.11		Odd Ready	•	Hi-Z		Even Ready			
Cell Bus Cycle 0/58 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	TX Frame	-														0					<i>(</i>	
	Cell Bus Cycle	0/58	-	2	က	4	വ	8-9	တ	10	11	12-14	15	16	17	18	19	20-24	25	26	₹ _}	



FIG. 19 (CONT.)

			0																	
			ı	1	<u> </u>		Ι													
Byte 27	Bytes 27-32	Byte 33	Byte 34	Byte 35	Bytes 35-40	Byte 41	Byte 42	Byte 43	Bytes 43-48	Byte 49	Byte 50	Byte 51	Byte 52	Byte 53	Byte 54	Byte 55	Byte 56		Hi-Z	
Byte 27	Bytes 27-32	Byte 33	Byte 34	Byte 35	Bytes 35-40	Byte 41	Byte 42	Byte 43	Bytes 43-48	Byte 49	Byte 50	Byte 51	Byte 52	Byte 53	Byte 54	Byte 55	Byte 56	0	First Byte of	next cell
			0				C	•								-				
			0		_							Grant					>			
	Z-iH		Odd Present		Hi-Z		Even Present		Hi-Z		Odd Stop			Hi-Z			Even Stop		Hi-Z	
																			_	
27	27-32	33	34	35	35-40	41	42	43	43-48	49	50	51	52	53	54	55	56	57	28/0	
	Byte 27	Byte 27 Hi-Z Bytes 27-32	Hi-Z Byte 27 Bytes 27-32 Bytes 33	Hi-Z Byte 27 Byte 27 Hi-Z Byte 27 Byte 27 Byte 37 Byte 33 Odd Present 0 0 Byte 34 Byte 34	Hi-Z Hi-Z Byte 27 Byte 27 Byte 37 Byte 37 Byte 33 Odd Present 0 0 Byte 34 Byte 35	Hi-Z Hi-Z Byte 27 Byte 27 Byte 27 Byte 32 Byte 33 Byte 33 Byte 33 Byte 33 Byte 33 Byte 34 Byte 35 Byte 35 Byte 35 Byte 35	Hi-Z Hi-Z Byte 27 Byte 27 Byte 27 Byte 32 Byte 33 Byte 33 Byte 33 Byte 33 Byte 33 Byte 34 Byte 35 Byte 35 Byte 35 Byte 35 Byte 35 Byte 35 Byte 41 Byte 41	Hi-Z Odd Present Odd Present Hi-Z Even Present Odd Present Byte 37 Byte 35 Byte 35 Byte 41 Byte 42	Hi-Z Hi-Z Hi-Z Odd Present Odd Present Develope 27 Byte 27 Byte 27 Byte 27 Byte 33 Byte 33 Byte 34 Byte 35 Byte 35 Byte 35 Byte 35 Byte 41 Byte 41 Byte 42 Byte 43 Byte 43	Hi-Z Hi-Z Odd Present Odd Present Even Present Hi-Z Hi-Z Byte 27 Byte 37 Byte 33 Byte 33 Byte 33 Byte 34 Byte 35 Byte 35 Byte 35 Byte 35 Byte 35 Byte 41 Byte 41 Byte 41 Byte 42 Byte 43 Byte 43 Byte 43 Byte 43 Byte 43	Hi-Z Hi-Z Odd Present Odd Present Odd Present Hi-Z Even Present Odd Present Odd Present Odd Present Odd Present Even Present Odd Present Odd Present Odd Present Odd Present Byte 33 Byte 33 Byte 33 Byte 34 Byte 35 Byte 41 Byte 41 Byte 42 Byte 43 Byte 43 Byte 43 Byte 43 Byte 49 Byte 49	Hi-Z Hi-Z Hi-Z Odd Present Odd Present Even Present Odd Stop Odd Stop Hi-Z Odd Stop Hi-Z Hi-Z Byte 27 Byte 37 Byte 33 Byte 33 Byte 34 Byte 35 Byte 35 Byte 35 Byte 41 Byte 41 Byte 41 Byte 42 Byte 43 Byte 43 Byte 43 Byte 43 Byte 43 Byte 49 Byte 49 Byte 50 Byte 50	Hi-Z Hi-Z Byte 27 Byte 27 Byte 37 Byte 33 Byte 33 Byte 33 Byte 33 Byte 33 Byte 34 Byte 35 Byte 35 Byte 41 Byte 41 Byte 42 Byte 42 Byte 42 Byte 43 Byte 49 Byte 49 Byte 49 Byte 49 Byte 50 Byte 50 Byte 51 Byte 51 Byte 51	Hi-Z Hi-Z Hi-Z Byte 27 Byte 27 Byte 33 Byte 33 Byte 33 Byte 33 Byte 33 Byte 33 Byte 33 Byte 33 Byte 33 Byte 35 Byte 35 Byte 41 Byte 41 Byte 42 Byte 43 Byte 43 Byte 49 Byte 49 Byte 50 Byte 50 Byte 50 Byte 51 Byte 52 Byte 52 Byte 50	Hi-Z Hi-Z Hi-Z Hi-Z Hi-Z Hi-Z Odd Present Dodd Present Even Present Fixed Present Codd Stop Grant Hi-Z Hi-Z Hi-Z Hi-Z Byte 27-32 Byte 37 Byte 33 Byte 33 Byte 33 Byte 33 Byte 35 Byte 35 Byte 42 Byte 42 Byte 42 Byte 43 Byte 43 Byte 43 Byte 49 Byte 50 Byte 50 Byte 50 Byte 51 Byte 52 Byte 53 Byte 51 Byte 52 Byte 53 Byte 53	Hi-Z Hi-Z Hi-Z Hi-Z Odd Present Odd Present Even Present Odd Stop Grant Hi-Z Hi-Z Byte 37 Byte 37 Byte 37 Byte 35 Byte 35 Byte 35 Byte 35 Byte 35 Byte 41 Byte 41 Byte 41 Byte 41 Byte 42 Byte 43 Byte 43 Byte 49 Byte 50 Byte 51 Byte 51 Byte 51 Byte 51 Byte 52 Byte 53 Byte 53 Byte 55 Byte 55 Byte 55 Byte 55 Byte 55	Hi-Z Hi-Z	Hi-Z Hi-Z	Hi-Z Hi-Z	Hi-Z Hi-Z



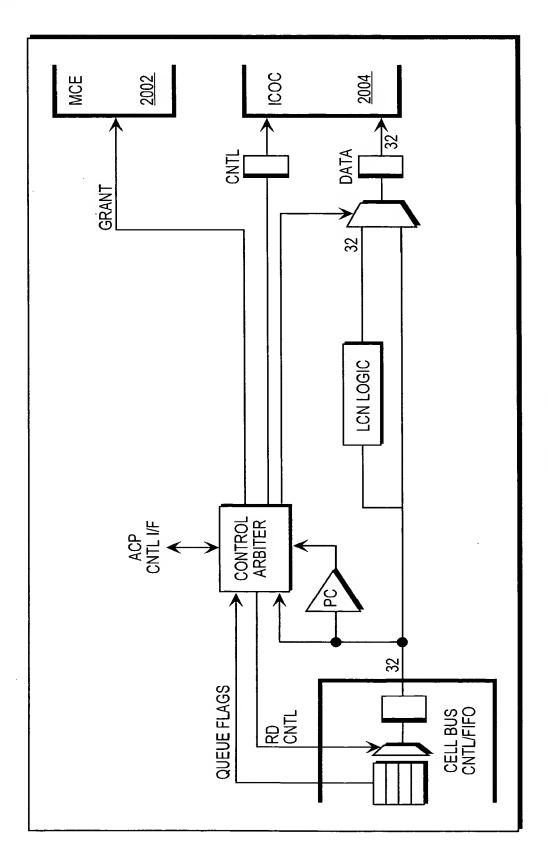


FIG. 20



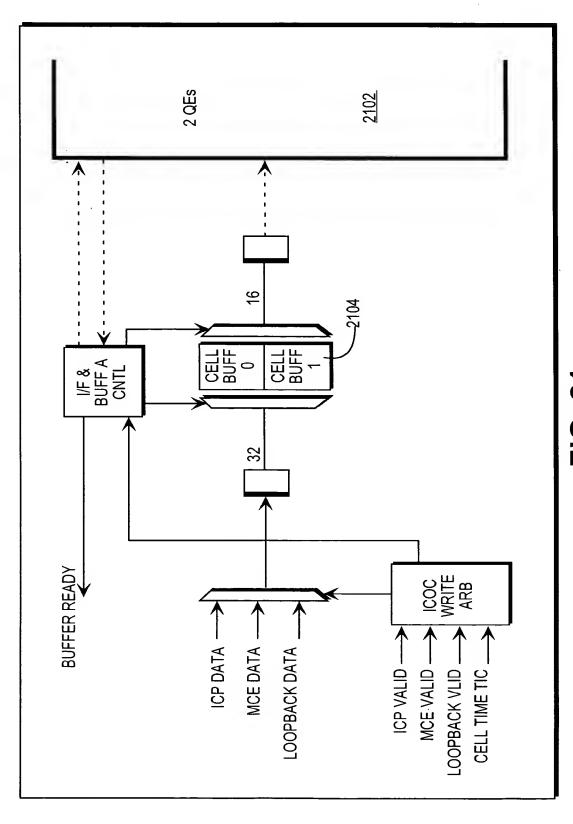


FIG. 21



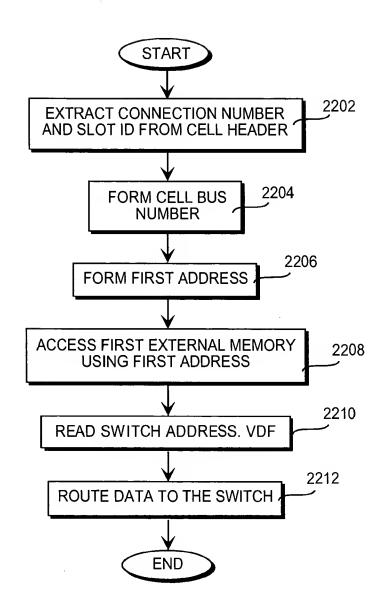


FIG. 22



Wo	2	TARGET	<u>.</u>	-	SLO	ا ا	,	. ~	> >	,	. 2	RESER	<u>≪</u>	
W						RESE	RVE							

TARGET ID - 0=CBM0, 1=CBM1, 2=CBM2, 3=CBM3, 4=MCE, 5=CBS

SLOT ID - CAN SPECIFY UP TO 8 SERVICE MODULES PER CELL BUS MASTER

V - VALID ENTRY

R, RESERVED - THESE BITS MUST BE SET TO ZERO



														/
RMATION	Address Map RAM (Addressed by the QE TX Address)	0x01	0x02	0x13	0x14	0x25	0x26	0x31	0x32	0x33	0x34	0x35	0×36	
CBC HARDWARE INFORMATION	QE Chip TX Address	0	-	2	က	4	2	9	7	ω	6	10	11	,
CBC HAF	CBC Chip Logic	CBM0	CBM0	CBM1	CBM1	CBM2	CBM2	CBM3	CBM3	CBM3	CBM3	CBM3	CBM3	\
	QE Chip Number	0	0	0	0	0	0	0	0	0	0	0	0	7
:	Physical Slot ID (on that Cell Bus)	1	2	3	4	5	9	1	2	3	4	5	9	
	Cell Bus Number	0	0	_	-	2	2	3	3	3	3	3	က	
RMATION	Chassis Slot Number	-	2	3	4	5	9	17	18	19	20	21	22	,
FIRMWARE INFORMATION	Comment	Fast or Slow SM	Slow SM only	7										
	Device	SM0	SM1	SM2	SM3	SM4	SM5	SM6	SM7	SM8	SM9	SM10	SM11	
	CBC Device Number	0	_	2	3	4	5	9	7	∞	တ	10	11	

FIG. 24



CBC HARDWARE INFORMATION	Address Map RAM (Addressed QE Chip by the QE TX Address Address)	12 0x40					NOT USED							Address Map RAM (Addressed by the QE	Address)
HARDWARE INFO	QE Chip TX Address	12												Adc Map (Addr by th	Adc
₹							13						14-15	QE Chip	I X Address
CBC	CBC Chip Logic	MCE	_				CBS						N/A	CBC Chip	Logic
	QE Chip Number	0					0						0	QE Chip	Number
	Physical Slot ID (on that Cell Bus)	N/A					N/A						N/A	Physical Slot ID	(on mar Cell Bus)
	Cell Bus Number	N/A					N/A				:		N/A	Cell Bus	MULIDE
ORMATION	Chassis Slot Number	N/A	8 for	PSM	Card in	Slot 7,		7 for	PSM	Card in	Slot 8		N/A	Chassis Slot	Number
FIRMWARE INFO	Comment	Internal to CBC			Internal to CBC	(RX is	Connected to	PSM in Slot 8,	TX is NOT	USED)			NOT USED	Comment	
	Device	MCE			•			Slave				Not	Nsed	Device	
	CBC Device Number	12					<u>.</u>					14-15		CBC Device	Number
	FIRMWARE INFORMATION	Device Comment Slot Number (on that Number Cell Bus)	Device Comment Slot Number (on that Number MME Internal to CBC N/A N/A N/A N/A N/A 0	Device Comment Slot Number (on that Number MCE Internal to CBC N/A N/A N/A N/A O	Device Comment Slot Number (on that Number MAE Internal to CBC N/A N/A N/A O BSM PSM	Device Comment Slot Number (on that Number Number R Number B Stor Bus) MCE Internal to CBC N/A N/A N/A 0 Internal to CBC Card in	Device Comment Slot Number (on that Number NIA NVA N/A N/A N/A N/A N/A N/A N/A N/A Slot Bus) REFINANWARE INFORMATION Chassis Slot ID Slot Internal to CBC N/A N/A N/A 0 REFINED REFINENCE Internal to CBC Card in (RX is Slot 7,	Device Comment Slot Number (on that Number PSM N/A N/A N/A O PSM PSM Slot To Card in (RX is Slot 7, N/A N/A N/A O Connected to Connecte	Device Comment Slot Number Cell Bus Slot ID CE Chip Number Cell Bus Slot ID CE Chip Number Cell Bus) Number PSM N/A N/A 0 PSM Slot 7, Connected to PSM in Slot 8, 7 for Slave PSM in Slot 8, 7 for Slave	Device Comment Slot Number Cell Bus Slot ID QE Chip Number Internal to CBC N/A N/A N/A N/A 0 RKX is Slot 7, Connected to Connected to Connected to CSM IT Slave PSM in Slot 8, 7 for TX is NOT PSM	Device Comment Slot Internal to CBC Card in (RX is Slave PSM in Slot 8) Connected to TX is NOT PSM USED) Chassis Cell Bus Slot ID QE Chip Number (on that Number Cell Bus) Rhysical Slot Internal to CBC	Device Comment Slot Internal to CBC Card in (RX is Slot 8) Connected to Connected to Slot 8 TX is NOT PSM USED) Card in Slot 8 Slot 8	Device Comment Slot ID Alber Solution Solution Number Number (on that Number Cell Bus) Number (on that Number Cell Bus) Number (on that Number Rym) Night Night Number Rym) Night Not Slot 8	Device Comment Slot Internal to CBC Aries Slot Internal to CBC Card in (RX is Slot 7, Connected to TX is NOT PSM USED) Card in USED) Card in Slot 8	Device Comment Slot Internal to CBC Card in (RX is Slot 8) Slave PSM in Slot 8 Connected to TX is NOT PSM USED) Comment Slot 7 Slave Comment Slot 8 Not Chassis Comment Slot 8 Not

FIG. 24 (CONT.)



	s Eed (2															읎	
RMATION	Address Map RAM (Addressed by the QE TX Address)	60×0	0x0	0x1B	0x1C	0x2D	0×2E	6E×0	YEX0	0x3B	0x3C	0x3D	0x3E	0x40		NOT USED	NOT USED
CBC HARDWARE INFORMATION	QE Chip TX Address	0	1	2	3	4	5	9	7	8	6	10	11	12		13	14-15
CBC HA	CBC Chip Logic	CBM0	CBM0	CBM1	CBM1	CBM2	CBM2	CBM3	CBM3	CBM3	CBM3	CBM3	CBM3	MCE		CBS	N/A
	QE Chip Number	_	1	1	-	-	1	1	-	1	1	1	1	1		1	1
	Physical Slot ID (on that Cell Bus)	6	10	11	12	13	14	6	10	11	12	13	14	N/A		N/A	N/A
	Cell Bus Number	4	4	5	5	9	9	7	7	7	7	7	7	N/A		N/A	N/A
RMATION	Chassis Slot Number	6	10	11	12	13	14	25	26	27	28	59	30	N/A		N/A	N/A
FIRMWARE INFORMATION	Comment	Fast or Slow SM	Slow SM only	Internal to CBC	Internal to CBC	NOT USED	NOT USED										
	Device	SM0	SM1	SM2	SM3	SM4	SM5	SM6	SM7	SM8	SM9	SM10	SM11	MCE		Slave	Not Used
	CBC Device Number	16	17	18	6	20	21	22	23	24	25	56	27	28		29	30-31



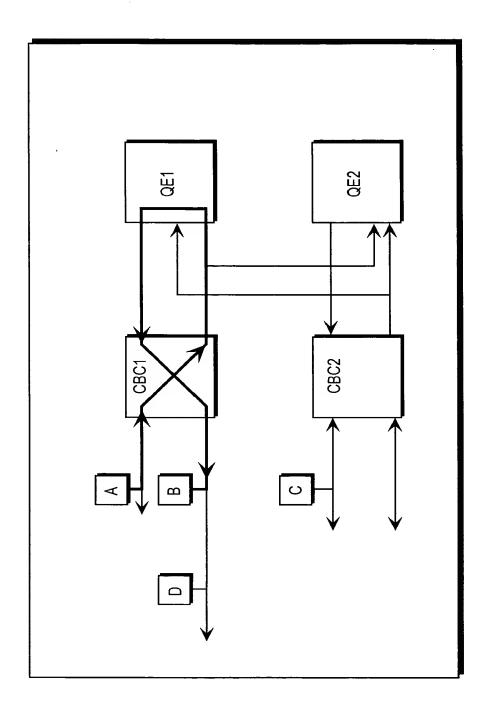


FIG. 26



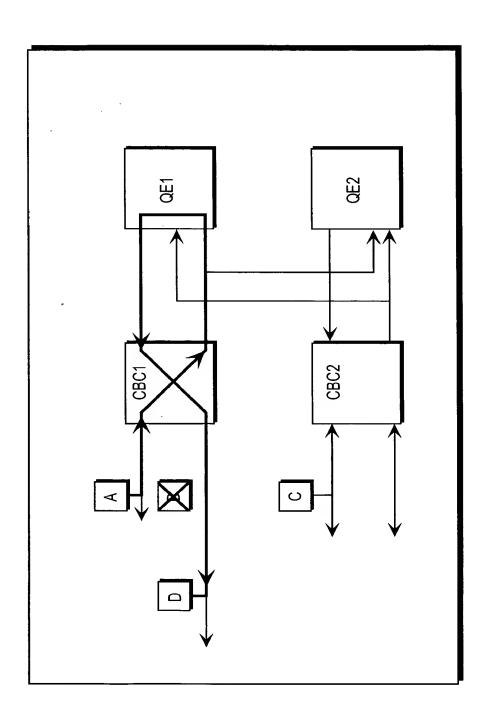


FIG. 27



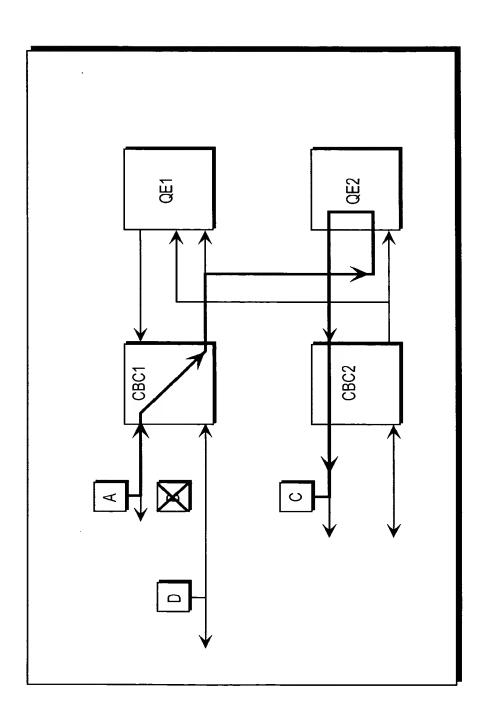


FIG. 28



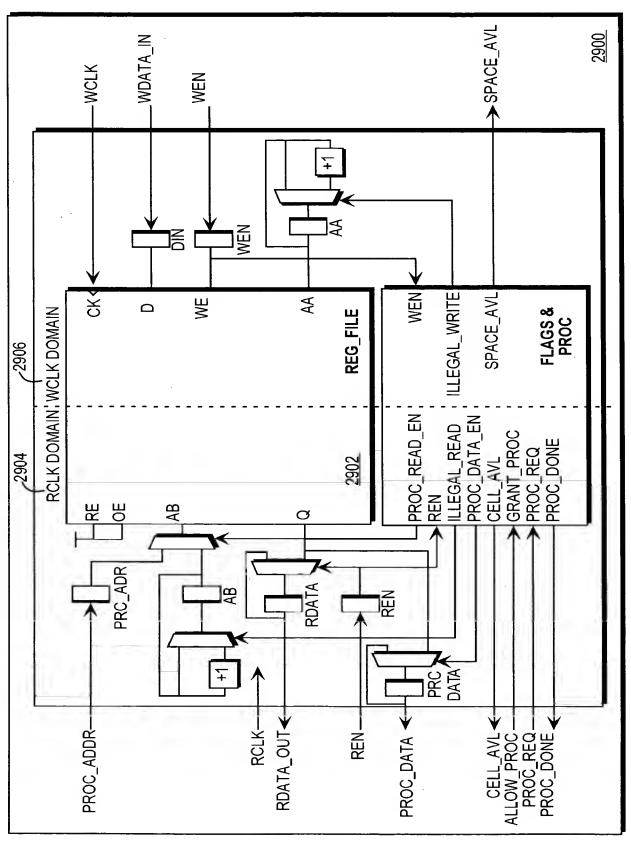


FIG. 29



PARAMETER	PURPOSE	CBM Egress FIFO	CBM Ingress FIFO	CBS Ingress FIFO
num_bits_in_fifo_word	Number of bits in each FIFO word	34	34	34
num_words_in_cell	Number of words in one cell	14	14	14
log2_num_words_in_cell	Minimum bits needed to represent num_words_in_cell	4	4	4
num_cells_in_fifo	Number of cells in the FIFO	8	8	16
log2_num_cells_in_fifo	Minimum bits needed to represent num_cells_in_fifo	3	3.	4
log2_num_words_in_fifo	Number of bits in FIFO address	7	7	8
wclk_2_rclk_ratio	WCLK to RCLK frequency ratio (minimum = 1) - WCLK=50 MHZ RCLK=21 MHZ RATIO=3 WCLK=21 MHZ RCLK=50 MHZ RATIO=1	3	_	_
rclk_2_wclk_ratio	RCLK to WCLK frequency ratio (minimum = 1) - RCLK=50 MHZ WCLK=21 MHZ RATIO=3 RCLK=21 MHZ WCLK=50 MHZ RATIO=1	_		3



NAME	COUNT	DIRECTION	COMMENTS
Write Port Interface			
write_clk_i	1	Input	Write Port Clock
wclk_reset_i		Input	Write Port Reset
write_data_i	num_bits_in_fifo_word	Input	Write Data Input
write_en_i	1	Input	Write Enable
write_cell_cntr_o	log2_num_cells_in_fifo	Output	Write Port Cell Count
cell_space_avail_o	1	Output	Room for at least one more cell
Read Port Interface			
read_clk_i	1	Input	Read Port Clock
rclk_reset_i	1	Input	Read Port Reset
read_data_o	num bits in fifo word	Output	Read Data Output
read_en_i		Input	Read Enable
read_cell_cntr_o	log2_num_cells_in_fifo	Output	Read Port Cell Count
cell_avail_o	-	Output	At least one more cell in FIFO
			Granting Processor Port for reading;
		Input	When the allow_proc_read_i is asserted,
			the Read Port is not allowed to read. In
allow_proc_read_i	_		addition, the next 2 cycles following the
			last cycle the allow_proc_read_i is
			asserted are also not available.
Processor Port Interface			



proc_read_req_i	-		
		Input	Processor request read operation
	log2_num_words_in_fifo	Input	Processor read address
proc_read_data_o num_bi	num_bits_in_fifo_word	Output	Processor read data
proc_read_done_o	1	Output	Processor read request completed
BIST Interface			
i_test_tsiq	1	Input	
bist_cntl_i	1	Input	
brt_flag_o	1	Output	
bist_complete_o	1	Output	

FIG. 31 (CONT.)



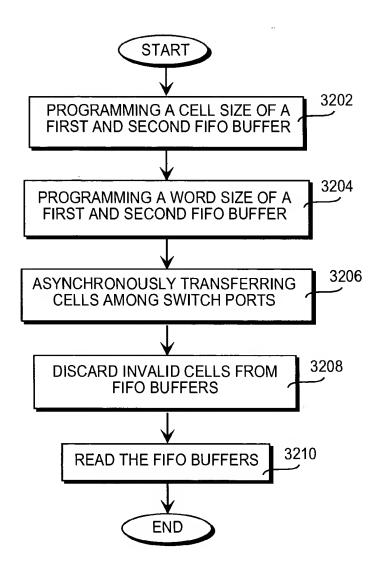


FIG. 32



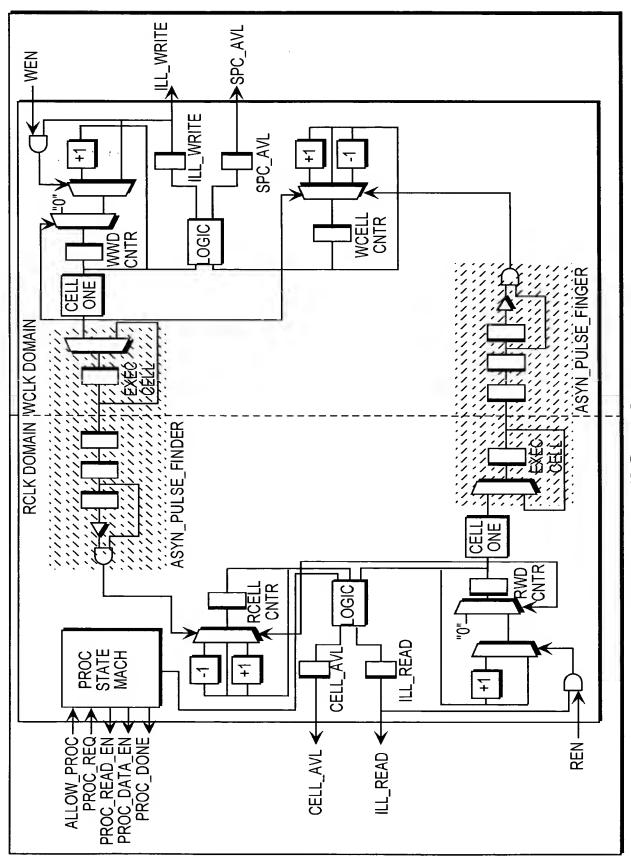


FIG. 33



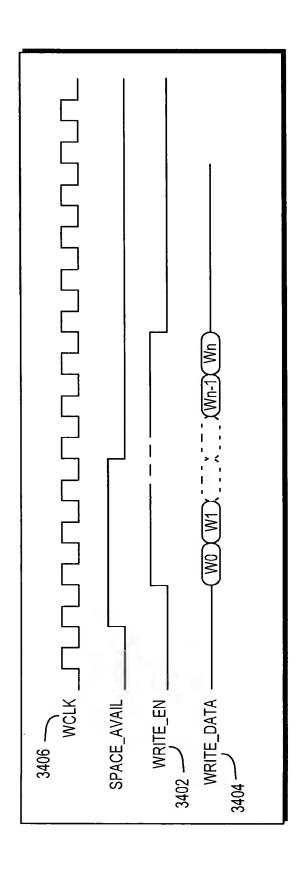


FIG. 34



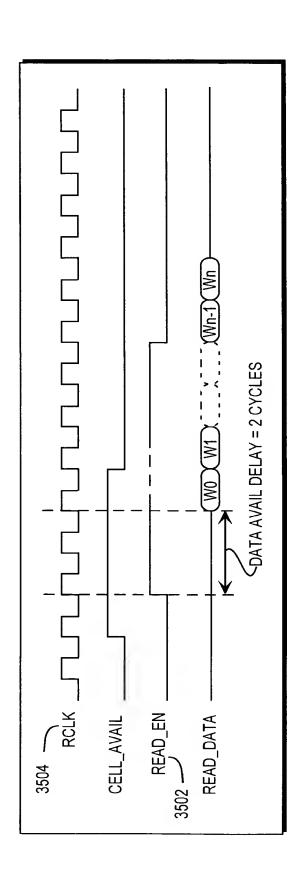


FIG. 35



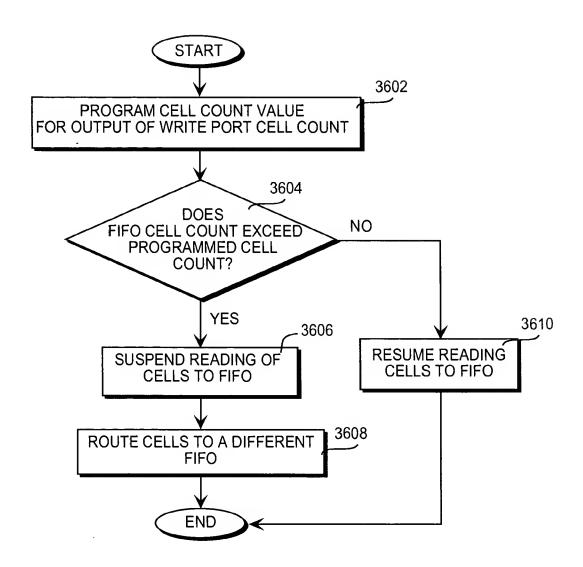


FIG. 36



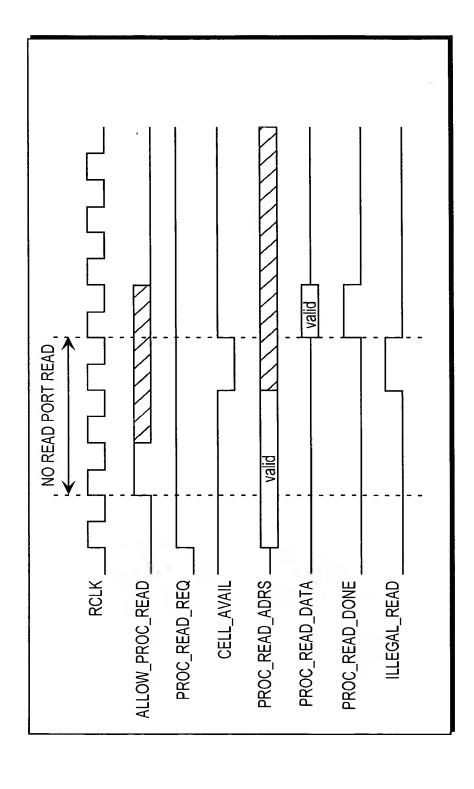


FIG. 37



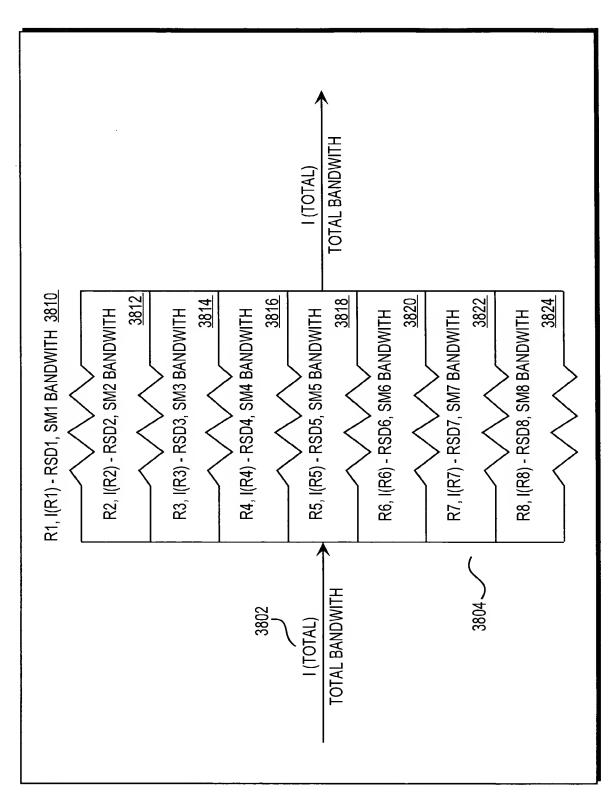


FIG. 38



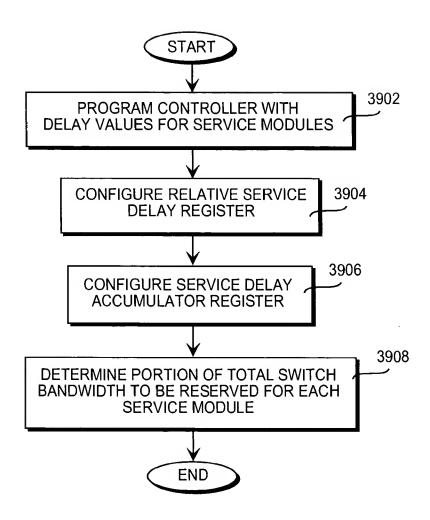


FIG. 39



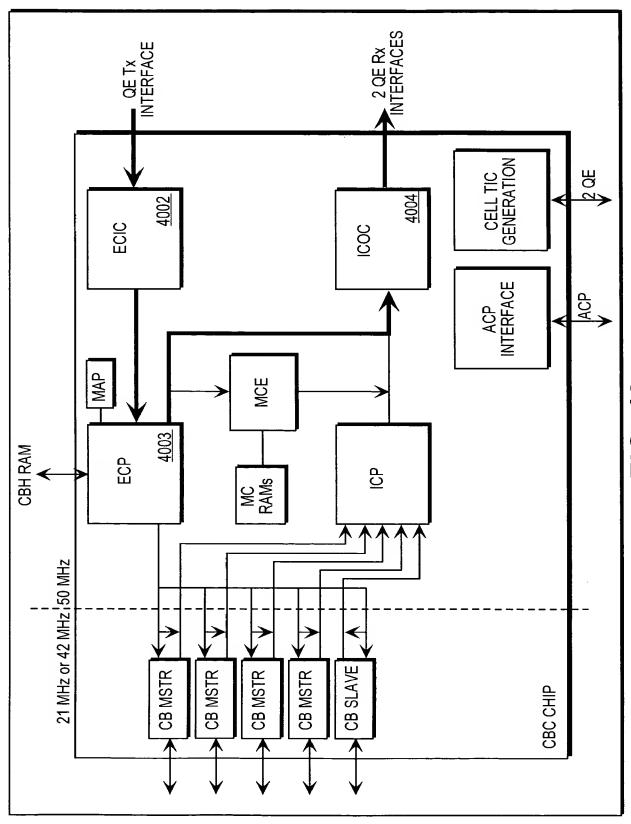


FIG. 40

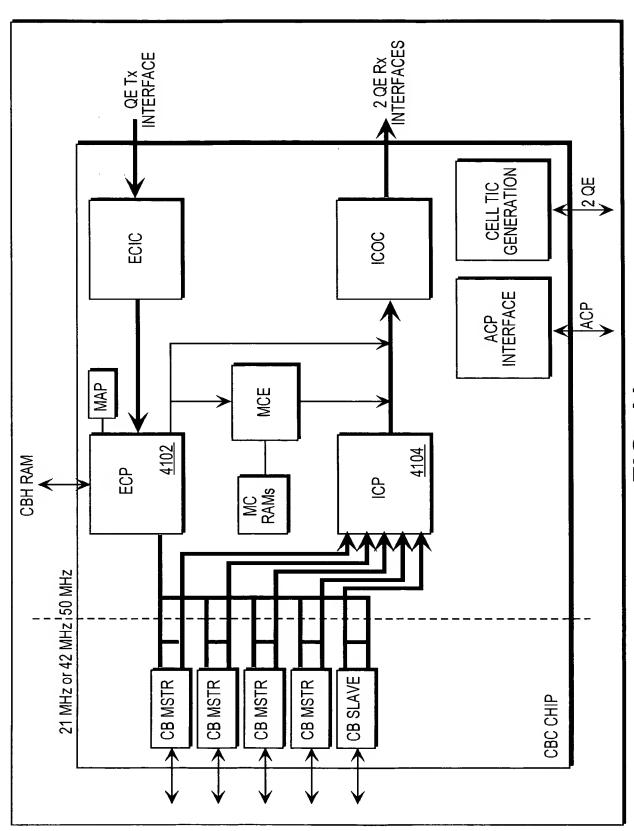


FIG. 41